# VLSI Testing

## Fault Modeling


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MEL G 626: VLSI Test & Testability

Lecture - 18

# Modified Yield Equation

- Three parameters:
  - Fault density, *f* = average number of stuck-at faults per unit chip area
  - Fault clustering parameter, β
  - Stuck-at fault coverage, *T*
- The modified yield equation:

$$Y(T) = (1 + TAf / \beta)^{-\beta}$$

Assuming that tests with 100% fault coverage (*T* =1.0) remove all faulty chips,

$$Y = Y(1) = (1 + Af / \beta)^{-\beta}$$

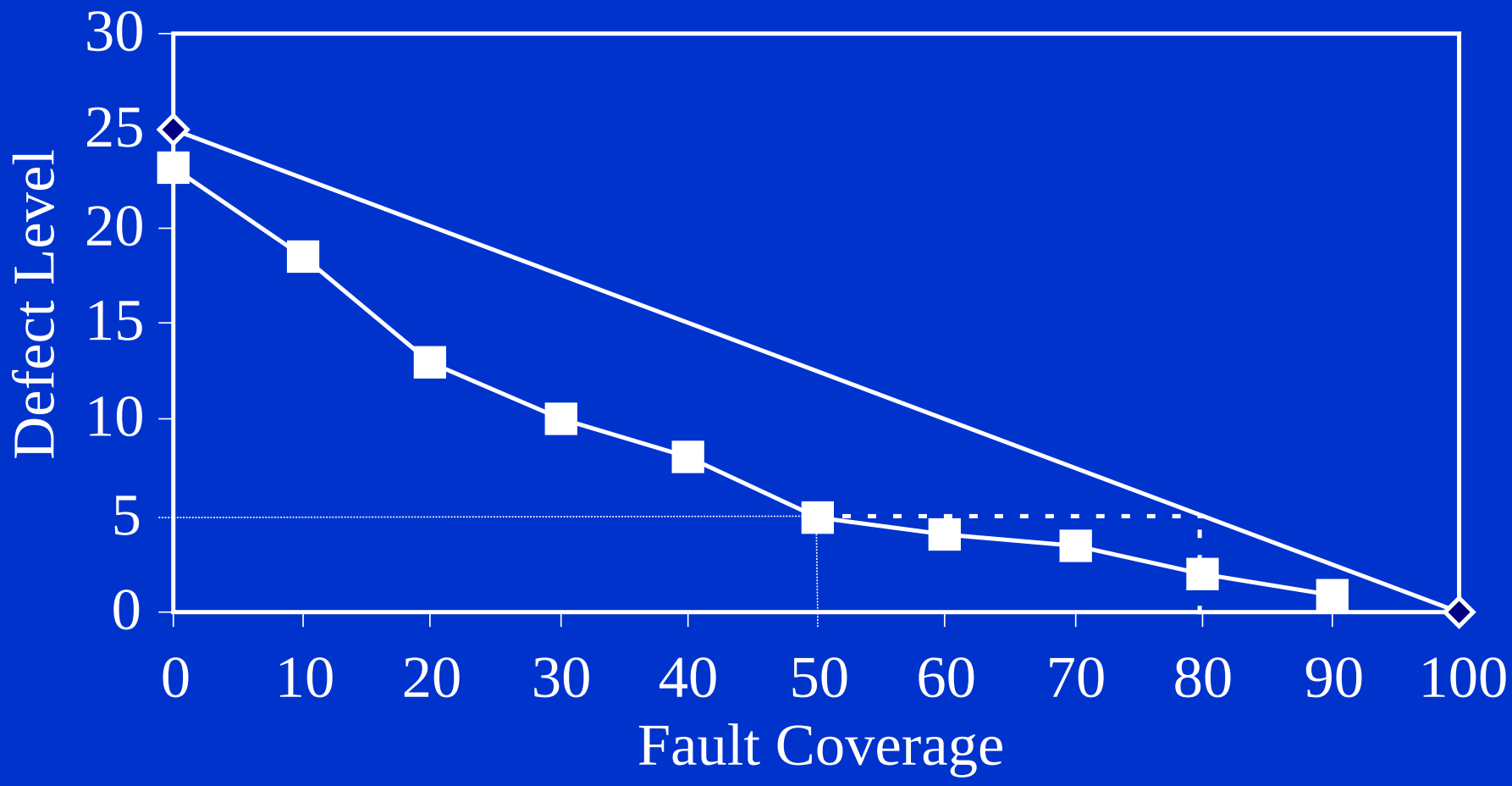
# Defect Level

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$

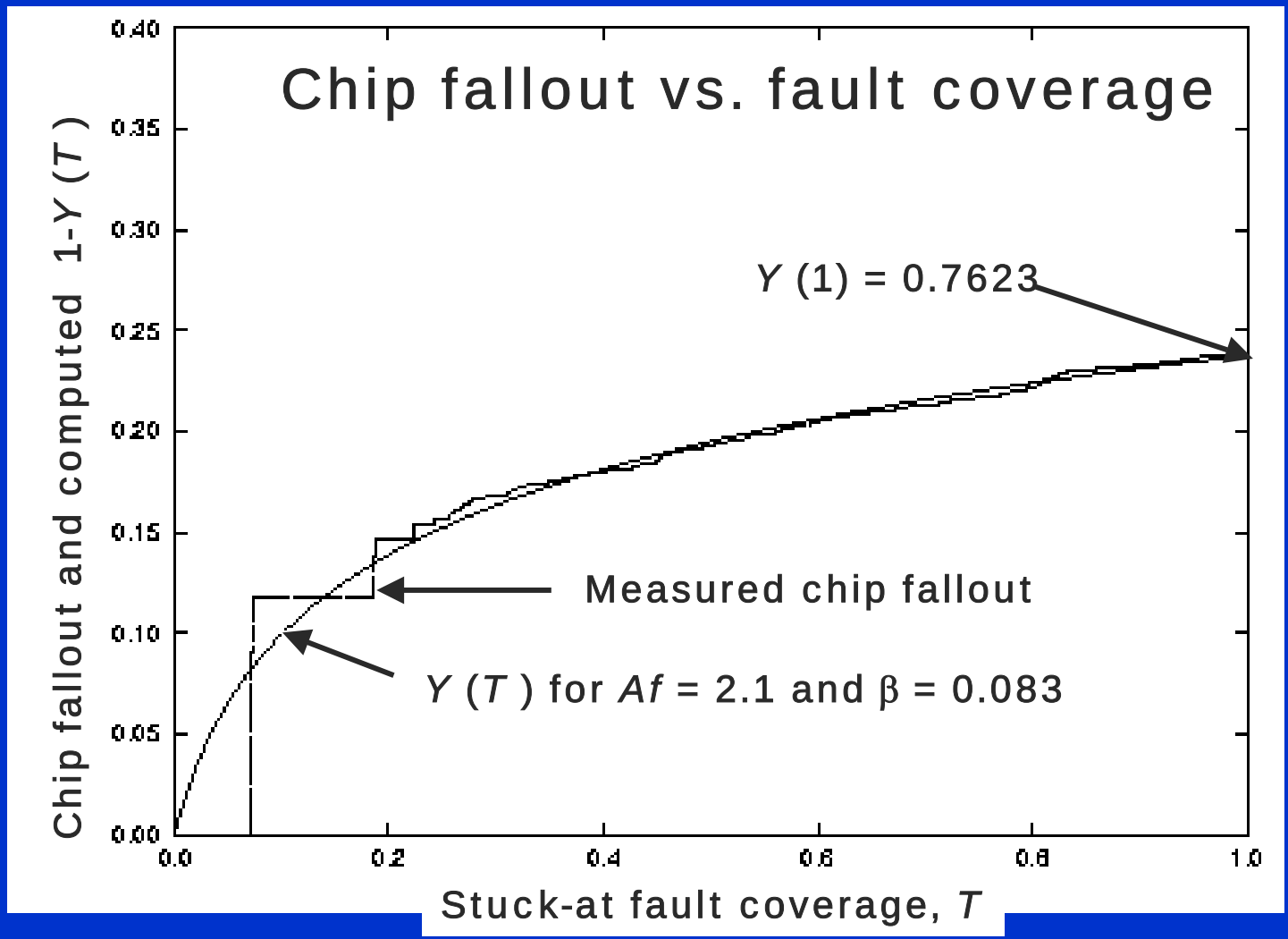
$$= 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$$

**Where $T$ is the fault coverage of tests, $Af$ is the average number of faults on the chip of area $A$, $\beta$ is the fault clustering parameter. $Af$ and $\beta$ are determined by test data analysis.**

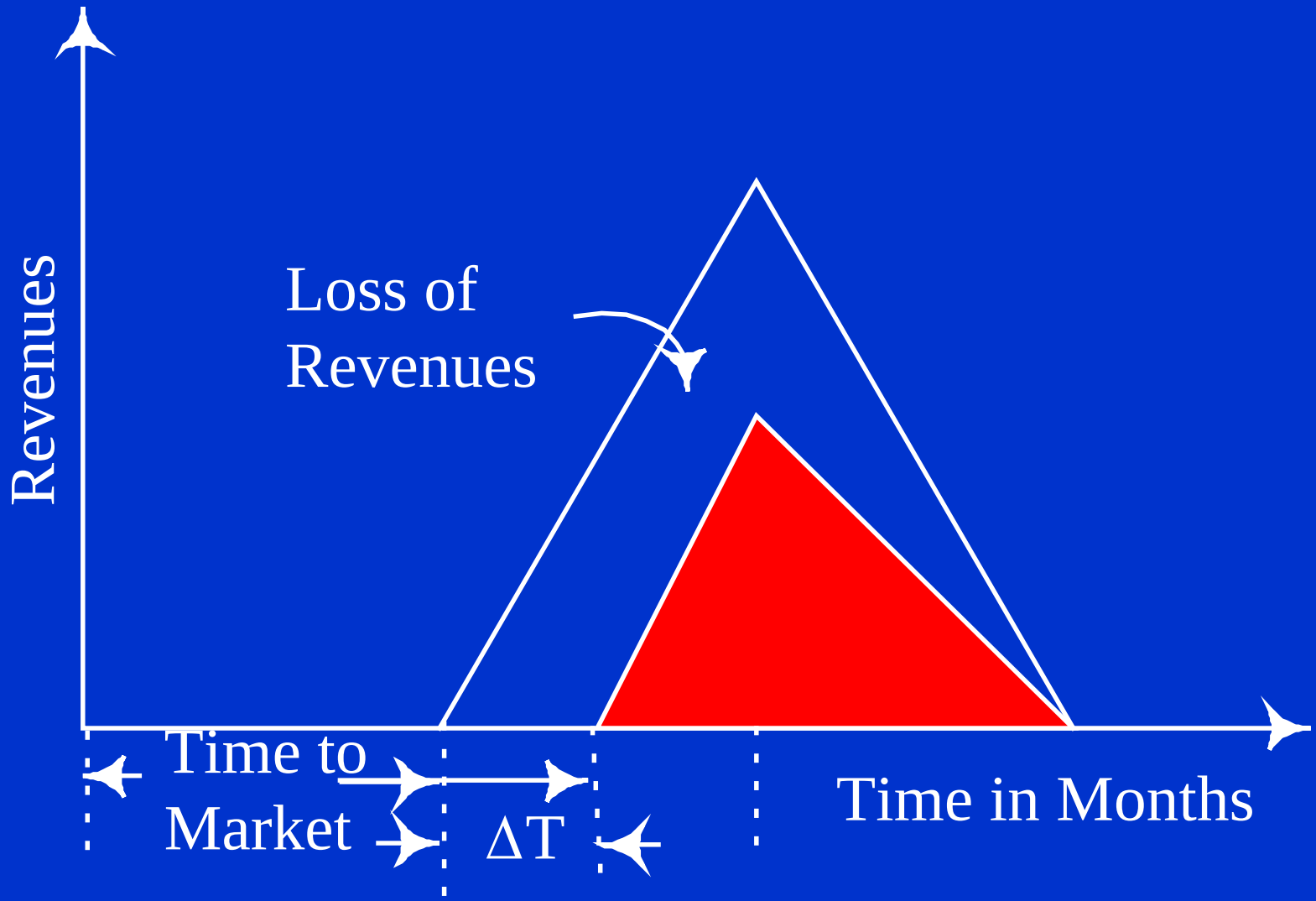
# Yield and Fault Coverage



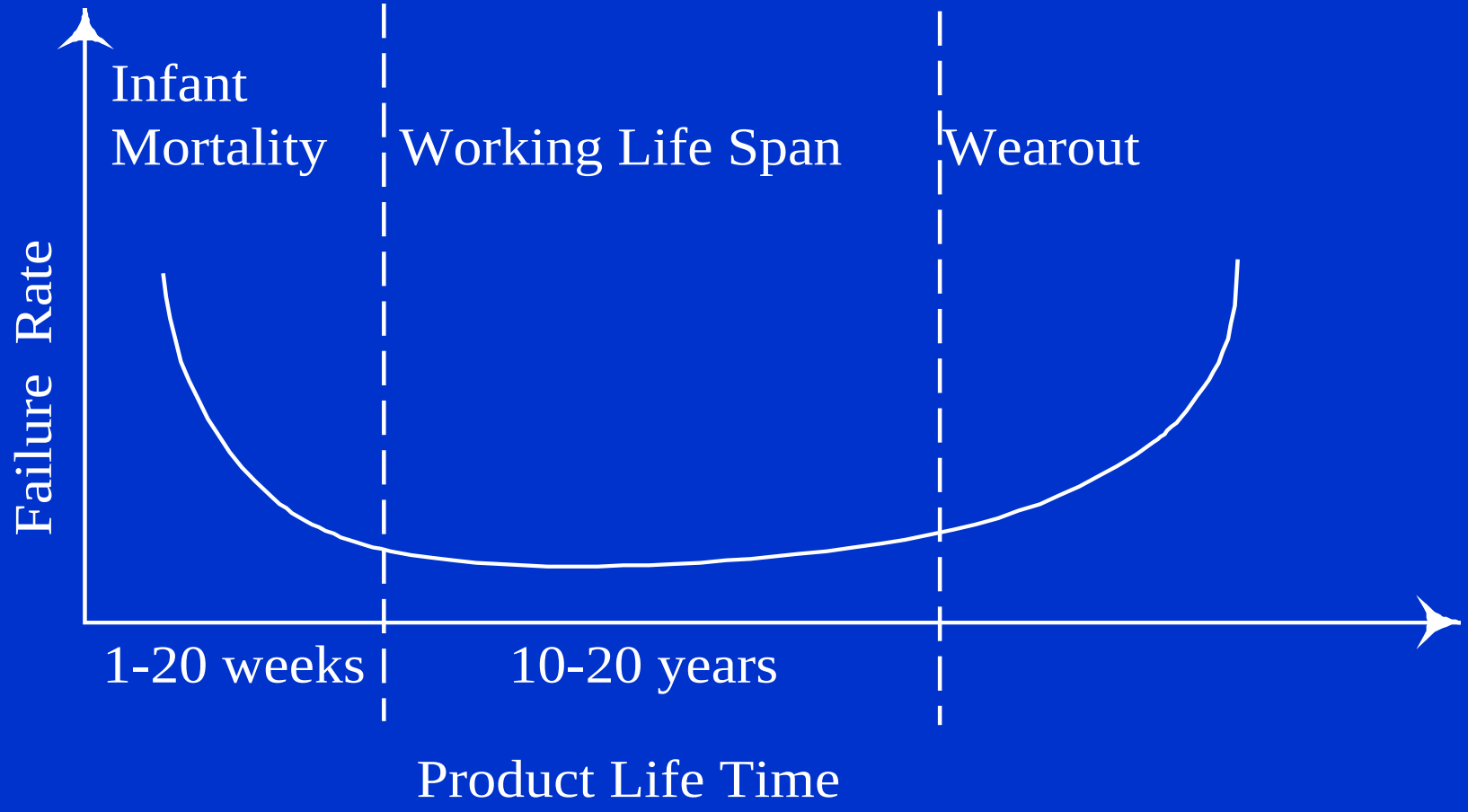
# Model Fitting



# Time to Market



# Failure Rate Vs Product Lifetime



# Definitions

- Defect: A defect in an electronic system is the unintended difference between the implemented hardware and its intended design
- Error: A wrong output signal produced by defective system is called error. An error is an effect whose cause is some defect
- Fault: A representation of a defect at the abstracted function level is called a fault

# Why Model Faults?

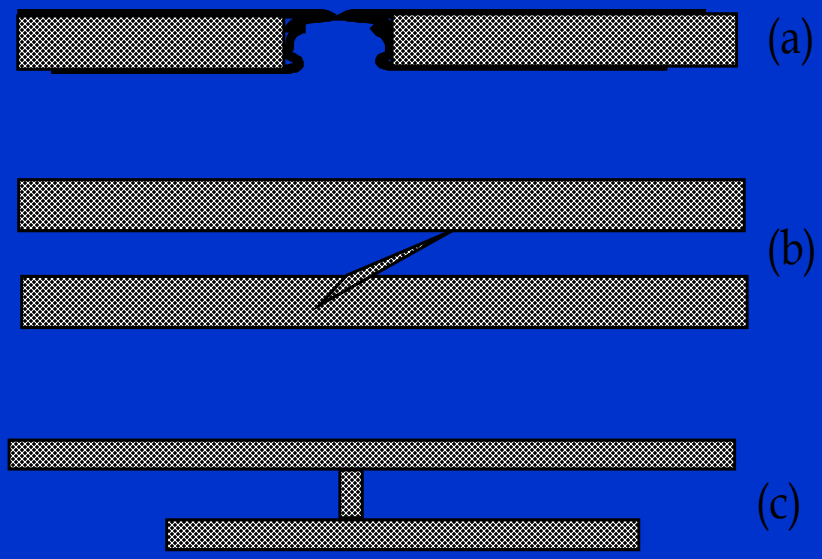
- I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing)
- Real defects (often mechanical) too numerous and often not analyzable
- A fault model identifies targets for testing
- A fault model makes analysis possible
- Effectiveness measurable by experiments

# Some Real Defects in Chips

- Processing defects
  - Missing contact windows
  - Parasitic transistors
  - Oxide breakdown
  - . . .
- Material defects
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - . . .
- Time-dependent failures
  - Dielectric breakdown
  - Electromigration
  - . . .
- Packaging failures
  - Contact degradation
  - Seal leaks
  - . . .

Ref.: M. J. Howes and D. V. Morgan, *Reliability and Degradation - Semiconductor Devices and Circuits,* Wiley, 1981.

# Electromigration

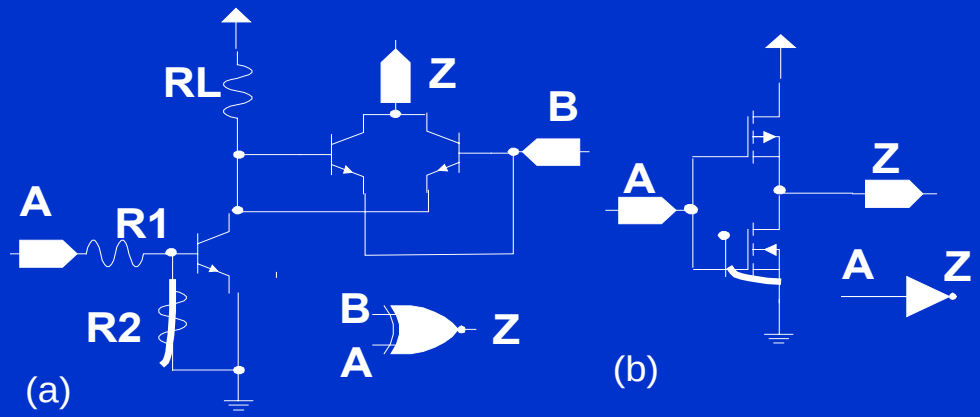



(a) Open in a line

(b) Short between two lines (whisker)

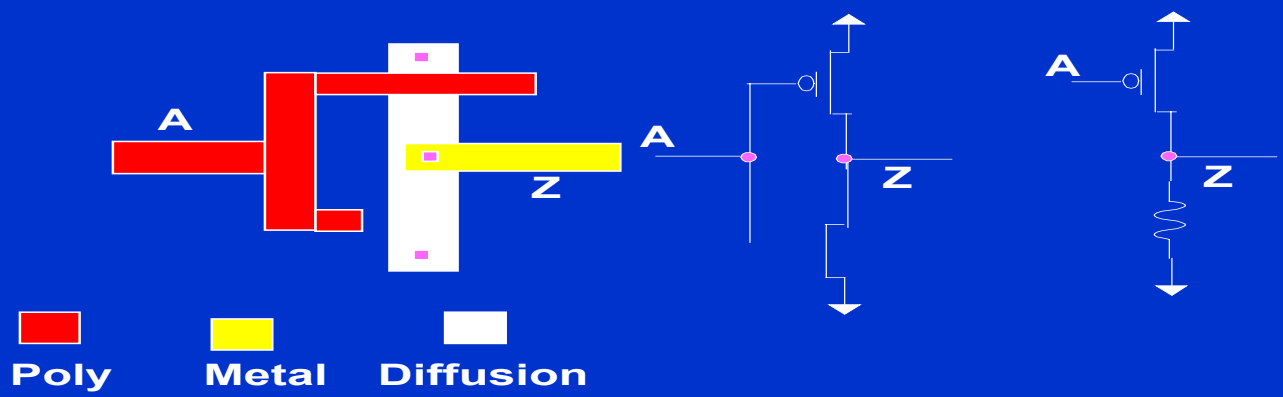
(c) Short between lines on different layers (hillock)

# Mapping Physical Defect into Faults 1



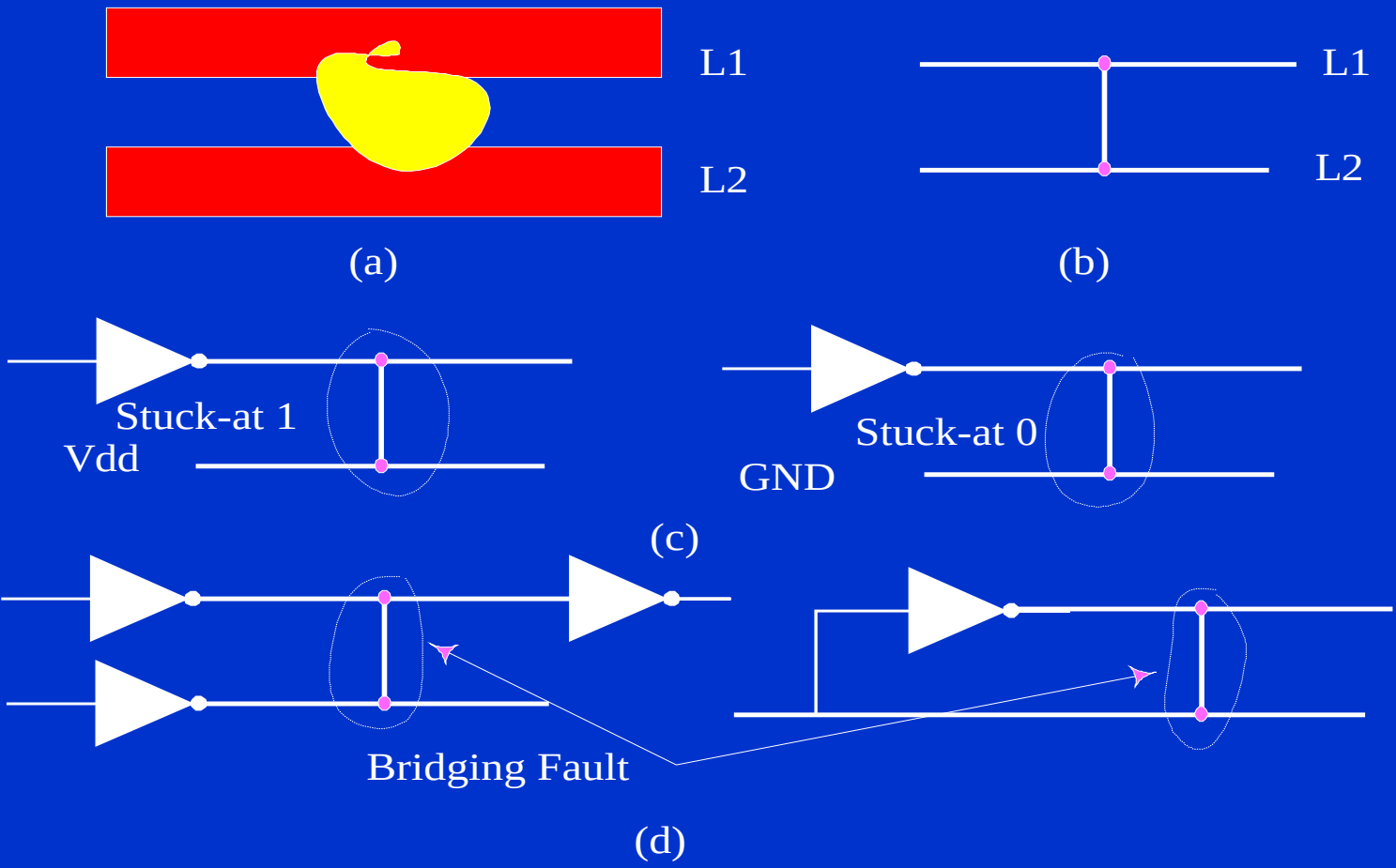

- Both the defective resistance in bipolar and a the oxide breakdown in oxide between the source and drain of the NMOS transistor form a short failure mode
- Both cases are mapped into a stuck-at fault

# Mapping Physical Defect into Faults 2




- Physical defect: A missing metal
  - NMOS is missing the gate
- Failure mode: an open
- Fault: open
- A possible circuit representation is shown

# Mapping Physical Defect into Faults 3

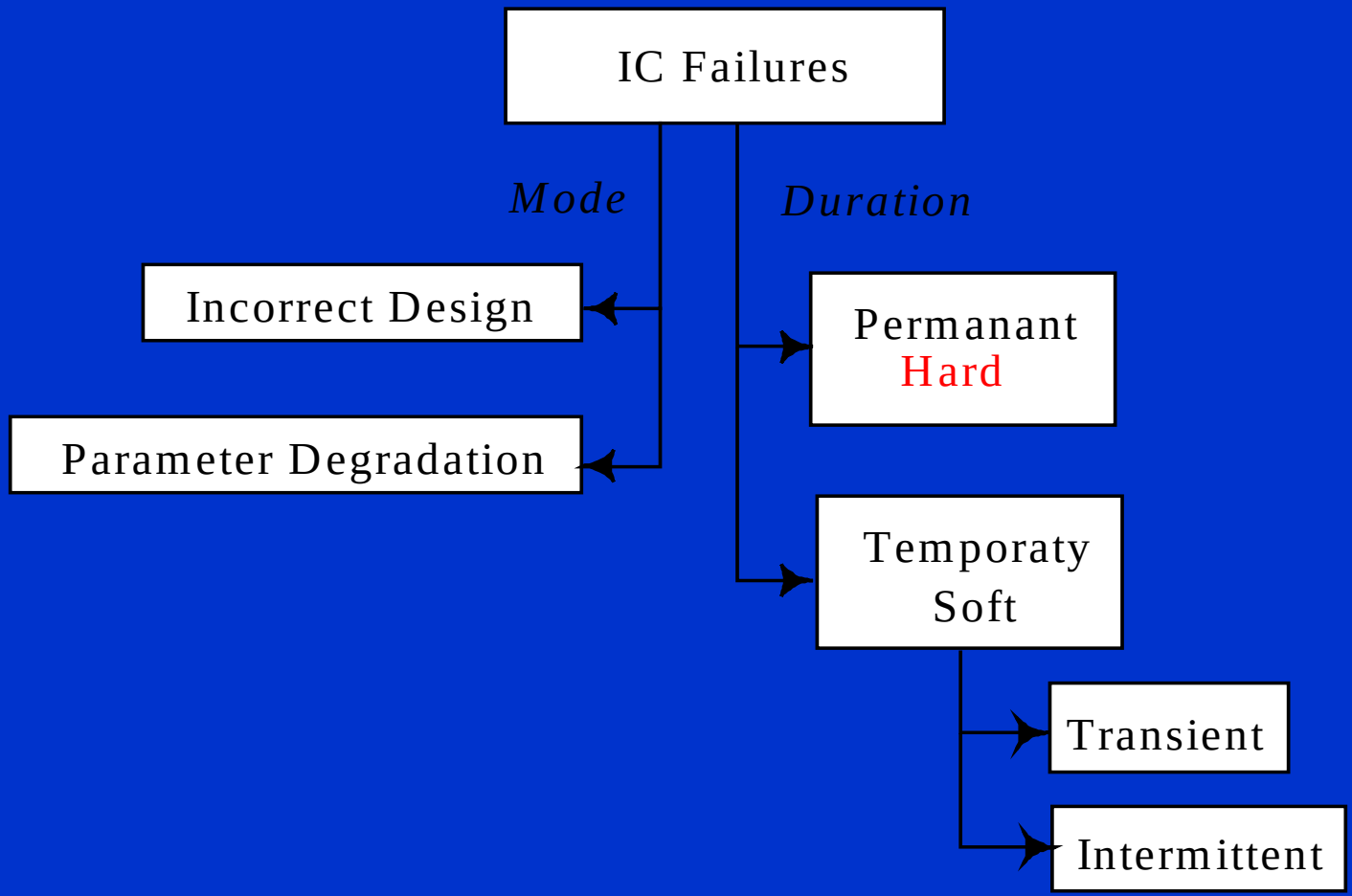


# Observed PCB Defects

| Defect classes | Occurrence frequency (%) |
|---|---|
| Shorts | 51 |
| Opens | 1 |
| Missing components | 6 |
| Wrong components | 13 |
| Reversed components | 6 |
| Bent leads | 8 |
| Analog specifications | 5 |
| Digital logic | 5 |
| Performance (timing) | 5 |

Ref.: J. Bateson, *In-Circuit Testing*, Van Nostrand Reinhold, 1985.

# Failure Classification

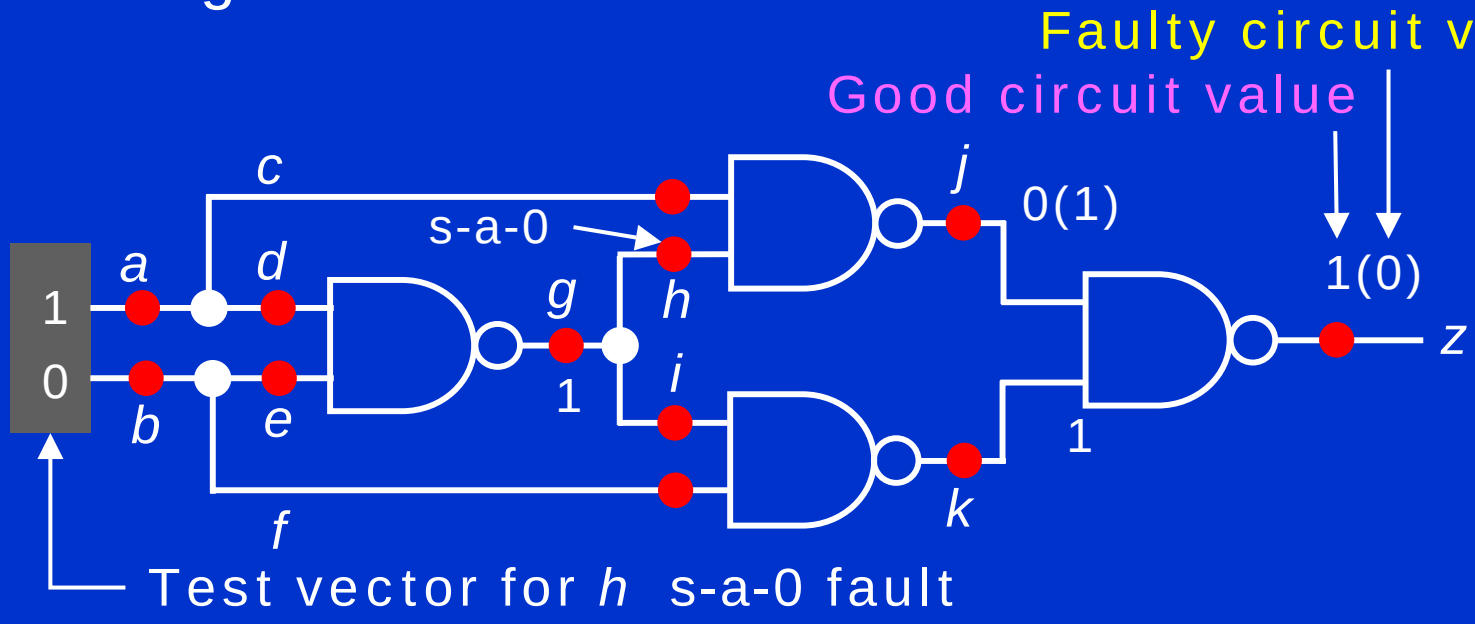


# Common Fault Models

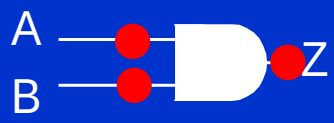
- Single stuck-at faults
- Transistor open and short faults
- Memory faults
- PLA faults (stuck-at, cross-point, bridging)
- Functional faults (processors)
- Delay faults (transition, path)
- Analog faults

# Single Stuck-at Fault

- Three properties define a single stuck-at fault
  - Only one line is faulty
  - The faulty line is permanently set to 0 or 1
  - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults

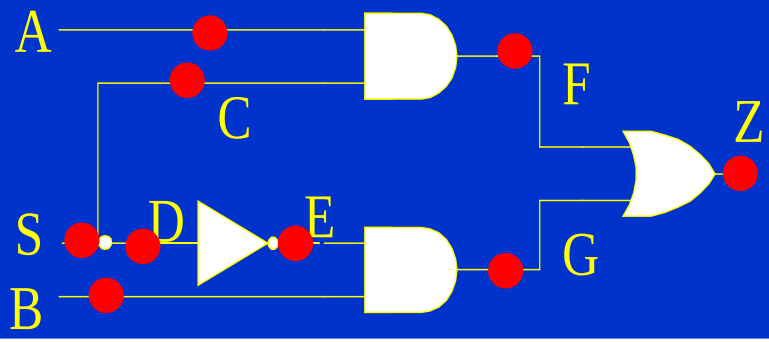


# SA Faults




| Inputs AB | FF Response | Faulty Response A/0 | B/0 | Z/0 | A/1 | B/1 | Z/1 |
|---|---|---|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 10 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 11 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

# SA Faults




| Inpu | Response | | | | | | |
|---|---|---|---|---|---|---|---|
| SAB | FF | S/0 | S/1 | C/0 | C/1 | *D*/0 | *D*/1 |
| 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 001 | 1 | 1 | **0** | 1 | 1 | 1 | **0** |
| 010 | 0 | 0 | **1** | 0 | **1** | 0 | 0 |
| 011 | 1 | 1 | 1 | 1 | 1 | 1 | **0** |
| 100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 101 | 0 | **1** | 0 | 0 | 0 | **1** | 0 |
| 110 | 1 | **0** | 1 | **0** | 1 | 1 | 1 |
| 111 | 1 | 1 | 1 | **0** | 1 | 1 | 1 |