VLSI Testing

Test Quality

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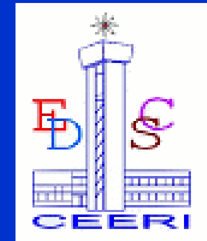
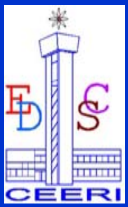


MEL G 626: VLSI Test & Testability

Lecture - 17



VLSI Realization Process

Customer's need

Determine requirements

Write specifications

Design synthesis and Verification

Test development

Fabrication

Manufacturing test

Chips to customer

Definitions

- ***Design synthesis:*** **Given an I/O function, develop a procedure to manufacture a device using known materials and processes.**
- ***Verification:*** **Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.**
- ***Test:*** **A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.**

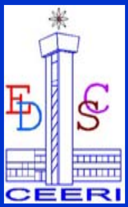
Verification vs. Test

Verification

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

Test

- Verifies correctness of manufactured hardware.
- Two-part process:
  1. Test generation: software process executed once during design
  2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.



Problems of Ideal Tests

- **Ideal tests detect all defects produced in the manufacturing process.**
- **Ideal tests pass all functionally good devices.**
- **Very large numbers and varieties of possible defects need to be tested.**
- **Difficult to generate tests for some real defects.** ***Defect-oriented testing is an open problem.***

Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*

Testing as Filter Process

Good chips

Prob(good) = y

Fabricated chips

Defective chips

Prob(bad) = 1- y

Prob(pass test) = high

Prob(fail test) = low

Prob(pass test) = low

Prob(fail test) = high

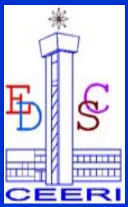
Mostly good chips

Tested chips

Mostly bad chips

Costs of Testing

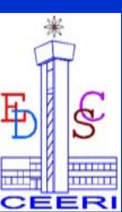
- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost



Present and Future*

	1997 -2001	2003 - 2006
Feature size (micron)	0.25 - 0.15	0.13 - 0.10
Transistors/sq. cm	4 - 10M	18 - 39M
Pin count	100 – 900	160 - 1475
Clock rate (MHz)	200 – 730	530 - 1100
Power (Watts)	1.2 – 61	2 - 96

** SIA Roadmap, IEEE Spectrum, July 1999*

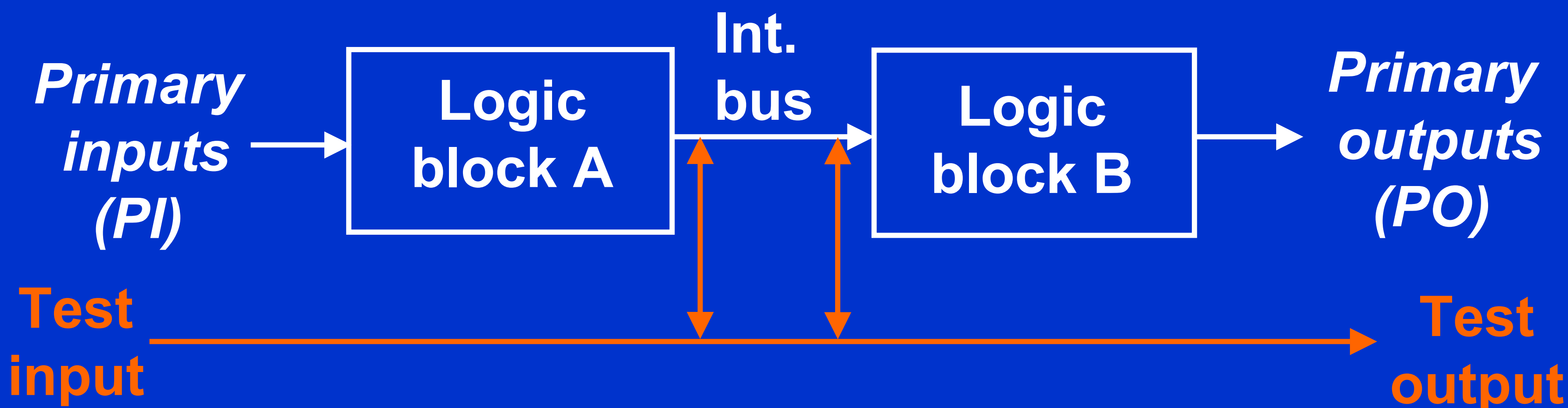


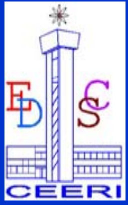
Design for Testability (DFT)

DFT refers to hardware design styles or added hardware that reduces test generation complexity.

Motivation: Test generation complexity increases exponentially with the size of the circuit.

Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.





Cost of Manufacturing Testing in 2000AD

- 0.5-1.0GHz; analog instruments; 1,024 digital pins: ATE purchase price

  = $1.2M + 1,024 x $3,000 = $4.272M

- Running cost (five-year linear depreciation)

  = Depreciation + Maintenance + Operation

  = $0.854M + $0.085M + $0.5M

  = $1.439M/year

- Test cost (24 hour ATE operation)

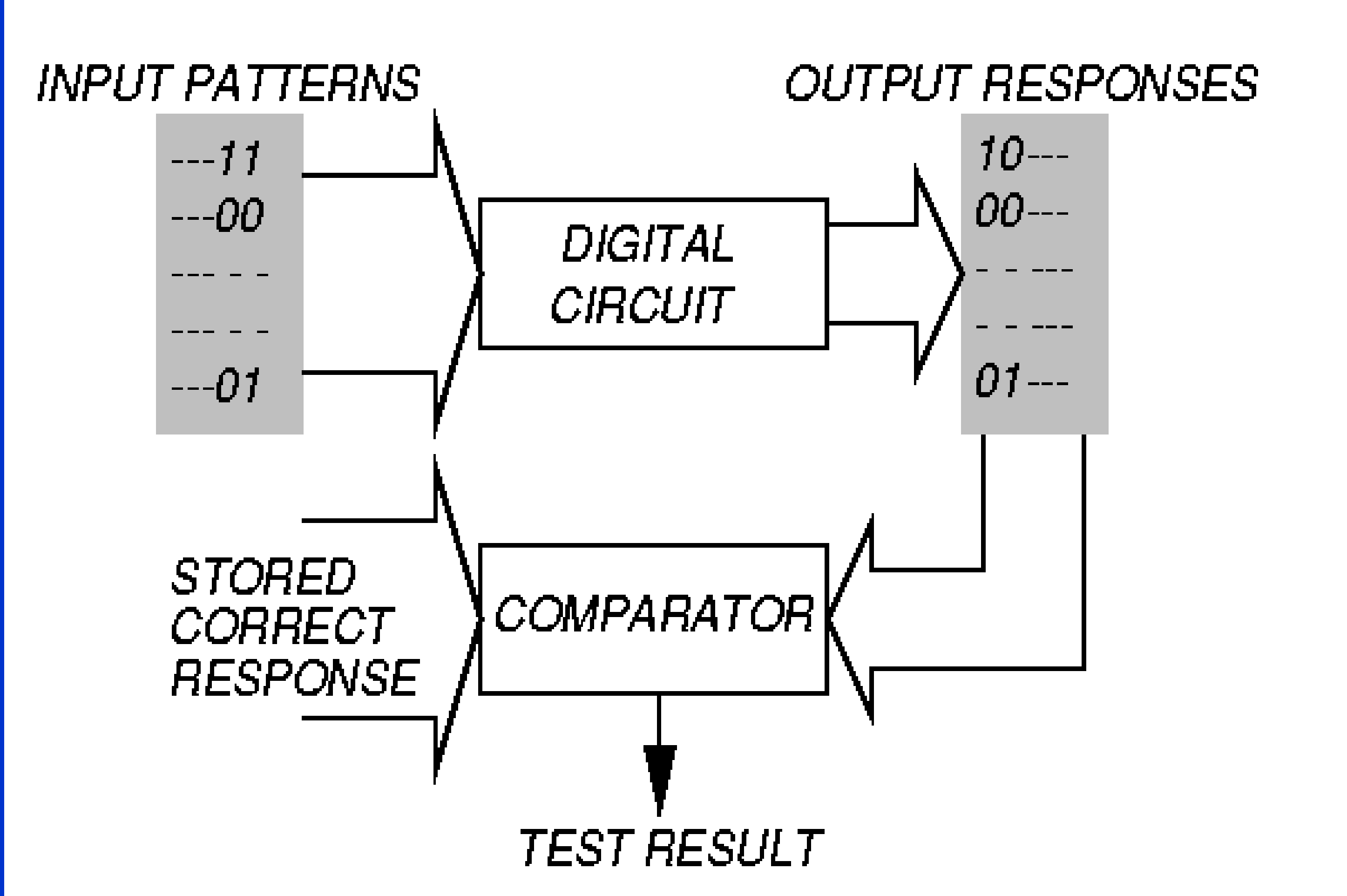
  = $1.439M/(365 x 24 x 3,600)

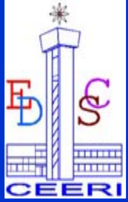
  = 4.5 cents/second

Roles of Testing

- **Detection**: Determination whether or not the *device under test* (DUT) has some fault.
- **Diagnosis**: Identification of a specific fault that is present on DUT.
- **Device characterization**: Determination and correction of errors in design and/or test procedure.
- ***Failure mode analysis*** (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

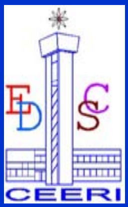
Testing Principle



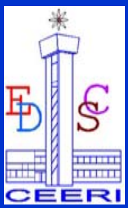


Automatic Test Equipment Components

- **Consists of:**
  - **Powerful computer**
  - **Powerful 32-bit *Digital Signal Processor* (DSP) for analog testing**
  - **Test Program (written in high-level language) running on the computer**
  - **Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)**
  - ***Probe Card* or *Membrane Probe* (contains electronics to measure signals on chip pin or pad)**



ADVANTEST Model T6682 ATE



T6682 ATE Specifications

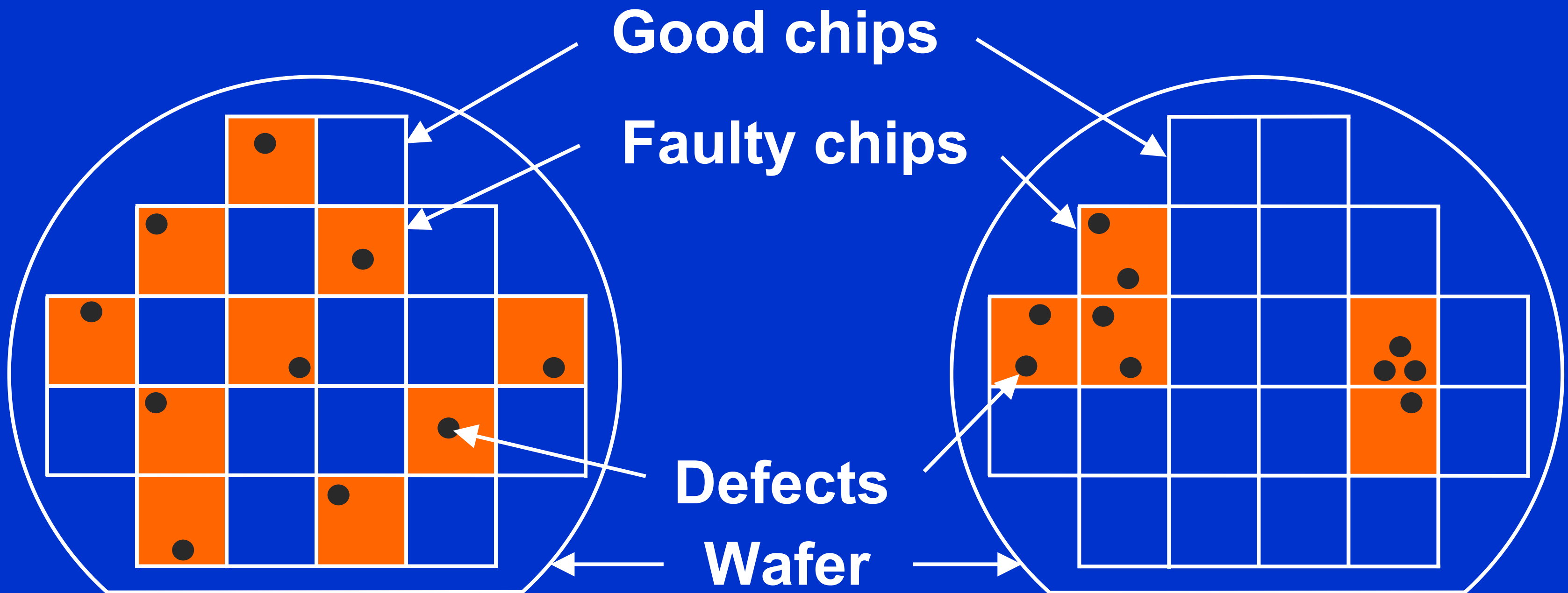
- **Uses 0.35 μm VLSI chips in implementation**
- **1024 pin channels**
- **Speed: 250, 500, or 1000 MHz**
- **Timing accuracy: +/- 200 ps**
- **Drive voltage: -2.5 to 6 V**
- **Clock/strobe accuracy: +/- 870 ps**
- **Clock settling resolution: 31.25 ps**
- ***Pattern multiplexing*: write 2 patterns in one ATE cycle**
- ***Pin multiplexing*: use 2 pins to control 1 DUT pin**

VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the ***yield***. Yield is denoted by symbol ***Y***.
- Cost of a chip:

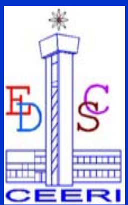
$$\frac{\text{Cost of fabricating and testing a wafer}}{\text{Yield x Number of chip sites on the wafer}}$$

Clustered VLSI Defects



Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77



Yield Parameters

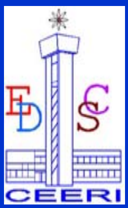
- Defect density (d) = Average number of defects per unit of chip area
- Chip area (A)
- Clustering parameter (α)
- Negative binomial distribution of defects,
  $p(x)$ = Prob (number of defects on a chip = x)

$$= \frac{\Gamma(\alpha+x)}{x!\,\Gamma(\alpha)} \cdot \frac{(Ad/\alpha)^{x}}{(1+Ad/\alpha)^{\alpha+x}}$$

where Γ is the gamma function

$\alpha = 0$, $p(x)$ is a delta function (maximum clustering)

$\alpha = \infty$, $p(x)$ is Poisson distribution (no clustering)



Yield Equation

Y = Prob (zero defect on a chip) = p (0)

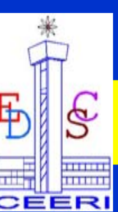
$$Y = (1 + Ad / \alpha)^{-\alpha}$$

Example: $Ad = 1.0$, $\alpha = 0.5$, $Y = 0.58$

Unclustered defects: $\alpha = \infty$, $Y = e^{-Ad}$

Example: $Ad = 1.0$, $\alpha = \infty$, $Y = 0.37$

too pessimistic !

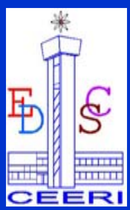


Defect Level or Reject Ratio

- *Defect level* (DL) is the ratio of faulty chips among the chips that pass tests.
- DL is measured as *parts per million* (ppm).
- DL is a measure of the effectiveness of tests.
- DL is a quantitative measure of the manufactured product quality. For commercial VLSI chips a DL greater than 500 ppm is considered unacceptable.

Determination of DL

- From field return data: Chips failing in the field are returned to the manufacturer. The number of returned chips normalized to one million chips shipped is the DL.
- From test data: Fault coverage of tests and chip fallout rate are analyzed. A modified yield model is fitted to the fallout data to estimate the DL.



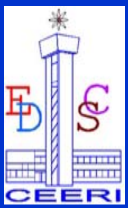
Modified Yield Equation

- Three parameters:
  - Fault density, f = average number of stuck-at faults per unit chip area
  - Fault clustering parameter, β
  - Stuck-at fault coverage, T
- The modified yield equation:

$$Y(T) = (1 + TAf / \beta)^{-\beta}$$

Assuming that tests with 100% fault coverage (T =1.0) remove all faulty chips,

$$Y = Y(1) = (1 + Af / \beta)^{-\beta}$$



Defect Level

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$

$$= 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$$

Where *T* is the fault coverage of tests, *Af* is the average number of faults on the chip of area *A*, β is the fault clustering parameter. *Af* and β are determined by test data analysis.