IEP on Technology CAD
(12-17\textsuperscript{th} May 2008)

VLSI Architecture Design

Presented By

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Basic VLSI Design Flow

- SYSTEM SPECIFICATION (Algorithmic Level)
- ARCHITECTURAL DESIGN (Register Transfer Level)
- LOGIC DESIGN (Gate Level)
- CIRCUIT DESIGN (Transistor Level)
- DEVICE DESIGN
- LAYOUT
- FABRICATION
- ON-WAFER TESTING
- PACKAGING
- CHIP TESTING

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Physical Design
Simulations at various levels

- SYSTEM SPECIFICATION  (Functional Simulation)
- ARCHITECTURAL DESIGN  (Block level Simulation)
- LOGIC DESIGN  (Logic Simulation)
- CIRCUIT DESIGN  (Circuit Simulation)
- DEVICE DESIGN  (Device Simulation)
- LAYOUT
- FABRICATION  (Process Simulation)
- ON-WAFER TESTING  (Fault Simulation)
- PACKAGING
- CHIP TESTING
OPTIMIZATION PROBLEM

PRIMARY OBJECTIVE FUNCTIONS

- SPEED
- AREA
- POWER

- The actual cost function involving these factors depends on specific application.
- Often they are considered to be constraint-satisfying problem rather than optimization problem.
- Design challenge is to have a better trade-off.
Concept of Hierarchy

- Continent
- Country
- State
- District
- City/Town/Village
- House
- Room
- Wall
- Brick

- System
- Subsystem
- Functional unit
- Functional subunit
- Flip flop/MUX/Adder
- Gate
- Transistor
- Device structure

... ...
TOP DOWN

ROOT NODE

LEAF CELLS

BOTTOM UP

DESIGN APPROACHES
FLOW OF CONSTRAINTS AND BACKANNOTATIONS

System Specification
(Speed, Area, Power etc.)

Constraint flow

Backannotation

Leaf cell parameters
( Characterization data )
A TYPICAL CHIP SHOWING CORE AREA AND PADS
A TYPICAL SEMICUSTOM CHIP USING STANDARD LIBRARY
A TYPICAL CUSTOM CHIP
Standard cell fishbone structure

$V_{DD}$

$p$-diff

$n$-diff

$V_{SS}$

Standard cell fishbone structure
Layout of a Standard Cell (2 input NAND gate)
OPTIMIZATION AT ALGORITHMIC LEVEL

EXAMPLE 1: DISCRETE FOURIER TRANSFORM (DFT)
O(N^2) [Unoptimized]

FAST FOURIER TRANSFORM (FFT)
O(N log N) [Optimized]

EXAMPLE 2: Sum of Natural Numbers

\[ S = 1 + 2 + 3 + \ldots + N \Rightarrow (N - 1) \text{ Additions} \]
\[ S = \frac{N(N + 1)}{2} \Rightarrow 1 \text{ Increment and 1 Multiplication} \]
( Division by 2 is a mere SHIFT in binary arithmetic )
OPTIMIZATION AT ARCHITECTURAL LEVEL

input N
S = 0
for i = 1 to N
    S = S + i
next i
output S

input N
S = 0
for i = N downto 1
    S = S + i
next i
output S
OPTIMIZATION AT LOGIC LEVEL

20 Transistors

14 Transistors

2:1 MULTIPLEXER
OPTIMIZATION AT CIRCUIT LEVEL

2:1 MULTIPLEXER USING TRANSMISSION GATE LOGIC

6 Transistors
(including 2 for inverting S)
Optimized transistor level realization of Boolean function

\[ Y = (AB + C)D \]

16 Transistors

8 Transistors
OPTIMIZATION WITH RESPECT TO VARIOUS OBJECTIVE FUNCTIONS

- **SPEED** @ LOGIC LEVEL

- **POWER** @ LOGIC LEVEL
**CMOS INVERTER**

**CMOS 2 INPUT NAND GATE**
CMOS INVERTER

CMOS 2 INPUT NAND GATE
CMOS INVERTER

CMOS 2 INPUT NAND GATE
APPLICATION SPECIFIC INTEGRATED CIRCUITS

- DIGITAL
- ANALOG
- MIXED SIGNAL
ANALOG VLSI

Where it differs from the Design with discrete components in a PCB or a breadboard?

• In the early days of Integrated Circuits:
  ⇒ absence of Capacitors

• At present:  ⇒ various constraints:
  Technology [CMOS]
  Area [e.g. in SoC]
  Noise [e.g. in mixed signal design]
ANALOG VLSI

- At present: 😞 various constraints:
  - Technology [CMOS]
  - Area [e.g. in SoC]
  - Noise [e.g. in mixed signal design]

😊 overall improvements:
- Higher Packing density
- Low Power consumption
- Higher Bandwidth
- High degree of Matching
ANALOG VLSI

Where do we stand today?

Thermionic Valve

Discrete Transistor

Integrated Circuits

- MSI
- LSI
- VLSI & beyond

- Millions of Transistors
- Deep Submicron Technology
- Quantum Devices (?)
ANALOG VLSI

☐ Challenges for Everyone:

• System designer
• Circuit designer
• Device designer
• Layout engineer
• Fabrication team
• Packaging people

❤ To push the performance limits
Resistors

- Diffusion resistors
- Polysilicon resistors
- $n$-well resistors
Concept of Sheet resistance
Sheet resistance (cont’d)
Sheet resistance (cont’d)
Capacitors

- Poly-to-diffusion capacitor
- Poly-to-poly capacitor
- Metal-to-poly capacitor
- Metal-to-metal capacitor
Issue of capacitor matching

\[
\frac{C_1}{C_2} = 1:4
\]
Issue of capacitor matching (cont’d)

\[ C_1 : C_2 = \frac{0.81}{3.61} = \frac{1}{4.45} \]
Issue of capacitor matching (cont’d)
Issue of capacitor matching (cont’d)

\[ C_1 : C_2 = \frac{0.81 \times 0.81}{4} = 1:4 \]
## Concept of Process corners

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<th>nMOS</th>
<th>pMOS</th>
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<tbody>
<tr>
<td>Fast</td>
<td>((V_T = 400 \text{ mV}))</td>
<td>Fast ((</td>
</tr>
<tr>
<td>Typ</td>
<td>((V_T = 500 \text{ mV}))</td>
<td>Typ ((</td>
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<tr>
<td>Slow</td>
<td>((V_T = 600 \text{ mV}))</td>
<td>Slow ((</td>
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## Concept of Process corners

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</tr>
</tbody>
</table>
Voltage gain: \( A_v = \frac{v_{out}}{v_{in}} = g_m R_L \)

\[
g_m = \frac{i_o}{v_{in}}
\]
\[ r_{DC} = \frac{v}{i} \quad r_{AC} = \frac{\partial v}{\partial i} \]
CMOS Amplifier with Active Load

CMOS Amplifier with Current Source Load

Push Pull CMOS Amplifier
Mobility could be different in different directions
Variations along $x$ and $y$ directions
Layout of Transistors for Differential Amplifier
CMOS Amplifier with Current Source (Active) Load

Voltage gain: 

\[ A_v = \frac{v_{out}}{v_{in}} = \frac{g_{mN}}{g_{dsN} + g_{dsP}} \]
CMOS Push Pull Amplifier

Voltage gain: \( A_v = \frac{v_{out}}{v_{in}} = \frac{(g_{mN} + g_{mP})}{(g_{dsN} + g_{dsP})} \)
It is interesting to note that the same circuit can work as an analog amplifier as well as a digital inverter.
Propagation delay of the \textit{digital inverter} fully depends upon the device parameters

\begin{align*}
t_{pLH} &= R_p \left( C_{\text{out}} + C_L \right) \\
t_{pHL} &= R_n \left( C_{\text{out}} + C_L \right)
\end{align*}
\[ v_{out} = (r_o \| R_L) g_m v_{in} \]

Low frequency model of an active device
$v_{\text{out}} = (r_0 \parallel R_L) g_m v_{\text{in}}$

Typical High frequency model of an active device
High frequency model of an active device and its corresponding frequency response

Introduces two poles: one corresponds to \((r_o | R_L)C_o\) and another \(r_s C_{in}\) \((r_s: \text{source resistance of the driver})\)
Conclusions

• Device Modeling and Process Modeling are extremely important in predicting the VLSI System Performance

• Quantum Devices are likely to take over the arena of VLSI Design in near future